Thermal Processing of Metal Alloys for an Improved CMP Process in Integrated Circuit Fabrication

Technical Field of the Invention

The present invention relates generally to integrated circuits and in particular the present invention relates to thermal processing for an improved CMP process.

Background of the Invention

As the density of semiconductor devices continues to increase, the need for smaller interconnections also increases. Historically, the semiconductor industry has used a subtractive etching process to pattern metal interconnect layers of the semiconductor. This metal processing technique, however, has limitations including poor step coverage, non-planarity, shorts and other fabrication problems. To address these problems, a dual damascene technique has been developed. This process, as explained in "Dual Damascene: A ULSI Wiring Technology", Kaanta et al., 1991 <u>VMIC Conference</u>, 144-150 (June 11-12, 1991) and incorporated herein by reference, involves the deposition of a metal into contact vias and conductor trenches which are patterned in the semiconductor. The semiconductor is then subjected to a known CMP (chemically-mechanically polish) process to both planarize the semiconductor and remove excess metal from all but the patterned areas.

The metal layer can be fabricated using known CVD (chemical vapor deposition) or PVD (physical vapor deposition) techniques. The metal interconnects are typically an aluminum alloys containing dopants, such as silicon and copper. These dopants are Si and Cu precipitates which tend to migrate to the grain boundaries of the aluminum during deposition. The precipitates are harder than aluminum. Thus, they are hard to dissolve and remove during the CMP process. The precipitates also contribute to defects in the aluminum, such as scratches, which materialize during the

CMP process. These problems are present in all CMP processes, and not limited to removing metal alloys used in a dual damascene process.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a process of fabricating metal alloy interconnects in an integrated circuit which improves a CMP process and reduces defects experienced during CMP.

Summary of the Invention

The above-mentioned problems with integrated circuit fabrication and other problems are addressed by the present invention and which will be understood by reading and studying the following specification. A thermal processing method is described which improves metal polishing and increases conductivity following polish.

In particular, the present invention describes a method of fabricating a metal layer in an integrated circuit. The method comprises the steps of depositing a layer of metal alloy which contains alloy dopant precipitates, performing a first anneal of the integrated circuit to drive the alloy dopants into solid solution, and quenching the integrated circuit to prevent the alloy dopants from coming out of solution. Excess metal alloy is then removed using a polish process, and a second anneal is performed after the excess metal alloy is removed to allow the dopants to come out of solution and increase a conductivity of the metal alloy.

In another embodiment, a method of fabricating a metal layer in an integrated circuit. The method comprises the steps of forming vias and interconnect trenches in the integrated circuit and depositing a layer of metal alloy which contains alloy dopant precipitates on the integrated circuit to fill the vias and interconnect trenches. A first anneal of the integrated circuit at 400 to 500° C to drive the alloy dopants into solid solution. The integrated circuit is quenched to prevent the alloy dopants from coming out of solution prior to removing excess metal alloy using a chemical-mechanical polish

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process. A second anneal at 150 to 250° C allows the dopants to come out of solution and increase a conductivity of the metal alloy.

A method of improving a chemical-mechanical polish (CMP) process in an integrated circuit is described. The method comprises the step of annealing the integrated circuit prior to performing the chemical-mechanical polish process to drive alloy dopants into solid solution.

A memory device is described which comprises an array of memory cells, internal circuitry, and metal contacts and interconnects coupled to the memory array and internal circuitry. The metal contacts and interconnects are formed by annealing the memory at a temperature sufficient to drive alloy dopants into solid solution prior to polishing the memory device to remove portions of a metal layer and form the metal contacts and interconnects.

Brief Description of the Drawings

Figures 1A- 1E are an illustration of a dual damascene fabrication technique according to the present invention; and

Figure 2 illustrates the basic process flow of the present metallurgy technique;

Figure 3 illustrates in more detail the dual damascene process of the present invention; and

Figure 4 is a block diagram of a memory device fabricated according to the present invention.

Detailed Description of the Invention

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and

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structural, logical, and electrical changes may be made without departing from the scope of the present invention. The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to include semiconductors, and the term insulator is defined to include any material that is less electrically conductive than the materials referred to as conductors. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

Prior to describing the process of the present invention, a description of the fabrication of metal conductor and contacts using a dual damascene process is provided. Referring to Figures 1A-E, a semiconductor base layer 100 is fabricated with an insulator layer 102, such as an oxide layer. The base layer is typically silicon having regions which are either p-type or n-type doped. A conductive area 104 is provided above the base layer. This conductive region can be any type of conductor or semiconductor, such as polysilicon, metal or doped silicon. A second layer of insulator material 106 is fabricated on top of the first insulator layer. Using known pattern and etch techniques, a contact via 108, or opening, is formed to access conductor area 104. A contact via 110 is also formed to access base layer 100. The vias may be tapered and are intended to provide access to any region or material which is desired to be coupled to a conductor interconnect.

Conductor interconnect trenches 112 are patterned and etched into the dielectric layer 106. After the trenches and access vias are formed, a layer of metal 114 (and necessary barrier metallurgy) is deposited on the device. A physical vapor deposition

technique, known to those skilled in the art, is used to fill the features and provide a layer of metal on top of layer 106. As known to those skilled in the art, a CMP process is implemented to remove excess metal from the top surface of the structure and provide defined interconnect lines 116.

In other integrated circuit fabrication processes (i.e., not dual damascene fabrication), the CMP step is provided to polish and planarize the integrated circuit wafer. The present invention improves the CMP process by providing a more uniform metal alloy for polishing.

During the metal deposition process, an aluminum alloy is deposited on the integrated circuit wafer along with dopants, such as copper and silicon. Aluminum has been typically used due to its low resistance and good adhesion to SiO_2 and Si. Silicon is usually added as an alloying element to alleviate junction spiking in Al contacts to Si. Further, electromigration and hillocks (spike-like formations) can be reduced by adding Cu, Ti, Pd or Si to aluminum to form alloys. These alloying elements precipitate at the grain boundaries. Thus, the grain boundaries are "plugged" and vacancy migration is inhibited.

The present invention is applicable to any precipitated material, but is particularly applicable to Al-Cu-Si alloys. In particular, Al-Cu, Al-Si and Cu-Si precipitates located at grain boundaries are not easily removed using standard CMP processes. This is primarily due to the hardness of the precipitates. Further, if a relatively large grouping of precipitates are experienced, damage in the form of scratches can occur to the aluminum interconnects during CMP.

Improved Interconnect Fabrication

The present invention provides a uniform metal alloy prior to performing a CMP process. That is, the metal layer is annealed in a conventional 400-500° C furnace to drive the precipitates dopants back into solution (i.e., a solid state reaction to force the Cu and Si to go back into solution). The wafer is then quenched to prevent formation of

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precipitate by driving the dopants out of solution. The result is a more uniform alloy material which can be more easily processed using known CMP techniques.

An undesirable side effect of annealing and quenching the alloy is a higher resistance of the interconnect. That is, the dopants are occupying states of the aluminum which causes interference in the flow of electrons across the metal. To reduce the resistance of the metal interconnects, the wafer is thermally soaked (i.e., 150-200° C anneal) such that the dopants form a second phase and then precipitate out, mainly at the grain boundaries. The reliability of the interconnect metal is also increased by reducing the electron drift which is enhanced by the presence of Si and Cu in solution. The two step thermal process is provided to both enhance the CMP process by providing a uniform alloy prior to CMP, and to improve the reliability and conductivity of the alloy after CMP by driving the dopants out of solution. Although some post-metal deposition annealing has been used in the past, the annealing is performed after a metal etch step to heal any plasma related damage which may be formed during fabrication and to react Al with underlaying layers to improve adhesion and electrical conductivity to underlying structures, not to enhance a subsequent CMP process.

While the anneal ranges 400-500° C and 150-250° C are intended for aluminum based alloys, the key is to provide a solid state reaction to drive precipitates into solution prior to a polish step. See Figure 2 for an illustration of the basic process flow of the present metallurgy technique. An integrated circuit is first fabricated with a layer of metal alloy which contains alloy dopant precipitates. The integrated circuit is annealed at 400 to 500° C to drive the dopants into solid solution. The integrated circuit is then quenched, using any known technique such as quenching in ambient air, to prevent the dopants from coming out of solution. The integrated circuit is then processed to remove excess metal alloy. It is preferred to use a chemical-mechanical polish process to remove the metal. After the circuit has been polished, a second anneal is performed at a lower temperature to allow the dopants to come out of solution. The conductivity of the metal alloy is thereby increased.

Figure 3 illustrates in more detail the dual damascene process of the present invention. A semiconductor base layer is fabricated with an insulator layer, such as an oxide layer. Using known pattern and etch techniques, contact vias are formed to access to any region or material which is desired to be coupled to a conductor interconnect. Conductor interconnect trenches are also patterned and etched into the dielectric layer. After the trenches and access vias are formed, a layer of metal alloy (and necessary barrier metallurgy) is deposited on the device. The integrated circuit is annealed at 400 to 500° C to drive the dopants into solid solution. The integrated circuit is then quenched, using any known technique such as quenching in ambient air, to prevent the dopants from coming out of solution. A CMP process is implemented to remove excess metal from the top surface of the structure and provide defined interconnect lines. After the circuit has been polished, a second anneal is performed at a lower temperature to allow the dopants to come out of solution. The conductivity of the metal alloy is thereby increased. It should be noted that the low temperature heat treatment is required to be performed only once. This process should be done after the last high temperature process.

MEMORY DEVICE

Figure 4 is a simplified block diagram of a memory device according to one embodiment of the present invention. The memory device 200 includes an array of memory cells 202, address decoder 204, row access circuitry 206, column access circuitry 208, control circuitry 210, and Input/Output circuit 212. The memory can be coupled to an external microprocessor 214, or memory controller for memory accessing. The memory receives control signals from the processor 214, such as WE*, RAS* and CAS* signals. The memory is used to store data which is accessed via I/O lines. It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device of Figure 4 has been simplified to help focus on the present invention. Thus, the memory includes internal circuitry and metal contacts and interconnects which are coupled to the memory array and internal circuitry.

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The metal contacts and interconnects are formed with an alloy of aluminum. The metal contacts and interconnects are formed by annealing the memory at a temperature sufficient to drive alloy dopants into solid solution prior to polishing the memory device to remove portions of a metal layer and form the metal contacts and interconnects. Specifically, a layer of metal alloy is deposited which contains alloy dopant precipitates. A first anneal of the memory is performed to drive the alloy dopants into solid solution. The memory is then quenched to prevent the alloy dopants from coming out of solution prior to removing excess metal alloy using a polish process. A second anneal of the memory is performed after the excess metal alloy is removed to allow the dopants to come out of solution and increase a conductivity of the metal alloy.

It will be understood that the above description of a DRAM is intended to provide a general understanding of the memory and is not a complete description of all the elements and features of a DRAM. Further, the present invention is equally applicable to any size and type of memory circuit and is not intended to be limited to the DRAM described above. Other alternative types of devices include SRAM or Flash memories. Additionally, the DRAM could be a synchronous DRAM commonly referred to as SGRAM, SDRAM, SDRAM II, and DDR SDRAM, as well as Synchlink or Rambus DRAMs.

Conclusion

A thermal processing method has been described which improves metal polishing and increases conductivity following polish. A method of fabricating a metal layer in an integrated circuit has also been described. The method comprises the steps of depositing a layer of metal alloy which contains alloy dopant precipitates, performing a first anneal of the integrated circuit to drive the alloy dopants into solid solution, and quenching the integrated circuit to prevent the alloy dopants from coming out of solution. Excess metal alloy is then removed using a polish process, and a second anneal is performed after the excess metal alloy is removed to allow the dopants to come out of solution and increase a conductivity of the metal alloy. The metal alloy can

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be aluminum with alloy dopants of silicon and copper where the first anneal is performed at 400 to 500° C. This process is particularly applicable to fabrication of interconnects formed using a dual damascene process. The integrated circuit has been described as any circuit, but can be a memory device such as a DRAM.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

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